REMARKS

Reconsideration of the present application is respectfully requested.

Objections to the Specification

The Examiner has objected to the disclosure because of a number of informalities. By this response Applicants have made the corrections suggested by the Examiner. In particular, the descriptions of Figs. 12-14 on page 8 have been amended to say that they show delay control circuits rather than power supply circuit. And the description on page 21, lines 12-14 has been amended to show that it refers to Fig. 8, not Fig. 3. No new matter has been added by these amendments.

In addition, Applicants have amended the specification on pages 13 and 14 to eliminate some extraneous text. In particular, the numbers 0031, 0032, 0033, and 0034 appeared as paragraphs on these pages and have been deleted by this amendment.

Based on these amendments to the specification, Applicants request that the Examiner withdraw the objection to the disclosure.

Claim Rejections - 35 U.S.C. § 102

The Examiner has rejected claims 1-5, 8-10, 13, 14, and 16-19 under 35 U.S.C. § 102(b) as being allegedly anticipated by United States Patent No. 5,625,279 to Rice et al. ("Rice").

By this response Applicants have cancelled claim 19 thus rendering moot this ground of rejection as it pertains to that claim.

Applicants have amended claim 1 to recite "a limited-current-value setting circuit setting a limited value to the output current, *wherein the limited value increases gradually over time during a rise of the output voltage up to the target voltage*," and "a current limiting circuit controlling the switching element to keep the detected output current at a current value less than or equal to the limited value during the rise of the output voltage up to the target voltage, *the current limiting control having priority over an output voltage tracking control*." Support for these amendments can be found, for example, on page 4, lines 9-29 of Applicants' specification. Rice does not disclose this combination of features.

As shown by this recitation, the current limiting circuit has priority over the voltage control circuit. This can be seen by way of example in Applicants' Fig. 2, which shows that the

transistor Q13, which is controlled by the current limiter 19, can shut off the transistors Q12 and Q11. (See, e.g., Applicants' specification, page 14, lines 20-30, and Fig. 2.)

The Examiner has asserted that the external controller in Figs. 2 and 8 of Rice shows the recited limited-current-value setting circuit, and that the oscillator in Figs. 2 and 8 of Rice shows the recited current limiting circuit. However, Rice teaches circuitry in which a controller 21 passes integers N1 and N2 as terminal counts to two coupled counters within an oscillator block 20. These counters are clocked with a 16 MHz system clock. The first counter is arranged to determine the duration of the HIGH output state of the oscillator signal appearing on line 23, while the second counter determines the duration of the LOW state of the signal. So, for instance, setting N1=58 and N2=6 would generate a 250 KHz, 90.6% duty cycle oscillator signal on line 23: 58P seconds HIGH and 6P seconds LOW, where P is the period of the 16 MHz system clock (62.5 nanoseconds). By varying the values of N1 and N2, a wide range of values of oscillator frequency and duty cycle can be generated, which values can be changed dynamically by controller 21. (See, e.g., Rice, from column 3, line 58, through column 4, line 6, and Fig. 2.)

But the control of switch Q1 is controlled by AND gate 85. The comparator 82 generates an over-current control signal when the voltage across current sense resistor 80 is greater than an offset voltage (typically 0.2 volts) applied by device 81. Comparators 87 and 88, with reference inputs "O-V" and "U-V", are responsible for generating control signals when Vout goes outside the over- or under-voltage limits, respectively. The signals from comparators 82, 87, and 88 are supplied to OR gate 83, whose output resets fault latch 84. The output of latch 84, when reset, turns off the drive to switch Q1, via AND gate 85. (See, e.g., Rice. column 6, lines 51-67, and Fig. 8.)

Nothing in this description, or any other portion of Rice discloses a limited-current-value setting circuit setting a limited value to the output current, *wherein the limited value increases gradually over time during a rise of the output voltage up to the target voltage*, and a current limiting circuit controlling the switching element to keep the detected output current at a current value less than or equal to the limited value during the rise of the output voltage up to the target voltage, *the current limiting control having priority over an output voltage tracking control.*

Claims 2-5, 8-10, 13, 14, and 16-18 all ultimately depend from claim 1 and are allowable for at least the reasons given above for claim 1.

Applicants have also amended claims 1-5, 8-11, 13, 14, and 16-18 to better recite the claimed invention. These additional amendments to claims 1-5, 8-11, 13, 14, and 16-18 are being made solely

to improve their readability and should not be considered as limiting the application of the doctrine of equivalents on these claims.

Based on at least the arguments given above, Applicant therefore respectfully requests that the Examiner withdraw the rejection of claims 1-5, 8-10, 13, 14, and 16-19 under 35 U.S.C. § 102(b) as being allegedly anticipated by Rice.

New Claims

By this response, Applicants have added new claims 20-28. Claims 20 and 21 depend from claim 1. Claims 22-28 recite a power supply circuit.

Although there are no pending rejections regarding claims 20-28, Applicants offer the following comments to distinguish independent claims 20-28 from the documents cited by the Examiner.

Claims 20 and 21 depend from claim 1 and are allowable for at least the reasons given above for claim 1.

New independent claim 22 recites "a limited-current-value setting circuit setting a limited value to the output current when a predetermined delay time has passed from an application of the input voltage to the input terminal, *wherein the limited value increases gradually with a progress in time during a rise of the output voltage up to the target voltage*," and "a current limiting circuit controlling the switching element to keep the detected output current at a current value less than or equal to the limited value during the rise of the output voltage up to the target voltage, *the current limiting control having priority over the output voltage tracking control*." It is allowable for reasons similar to those given above for claim 1.

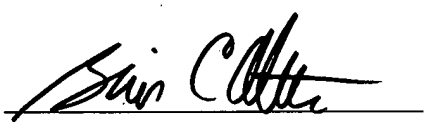
Accordingly Applicants submit that the pending claims in this application are not anticipated by Rice.

Conclusion

In view of the foregoing, Applicants respectfully submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

Please charge any unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,



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